REMARKS/ARGUMENTS

Favorable consideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-23 are pending in the application, with Claims 1, 9, 15, and 17 amended by the present amendment.

In the outstanding Office Action, the drawings were objected to; Claims 1-19 were rejected under 35 U.S.C. § 112, second paragraph; and Claims 1, 4, 6-7, 9-10, 12, 14-15, 17-18 and 20-23 were rejected under 35 U.S.C. § 102(e) as being anticipated by Park et al. (U.S. Patent No. 6,373,902 B1, hereinafter Park). Applicants submit that original Claims 2-3, 5, 8, 11, 13, 16, and 19 contain allowable subject matter since no basis for rejection of these claims under 35 U.S.C. § 102 or 103 was provided in the Official Action.

Applicants traverse the rejection of Claim 21 under 35 U.S.C. § 112, second paragraph, and note that Claim 20 provides antecedent basis for the term "modified inphase and quadrature data." Applicants also traverse the rejection of independent Claim 14 under 35 U.S.C. § 112, second paragraph, as no basis for this rejection is provided in the Official Action.

Applicants have amended Claims 1, 9, 15, and 17 to recite that "at least one lookup table containing ... modified inphase and quadrature bit patterns that do not cause overshoot." Support for this amendment is found in Applicants' originally filed specification.[1] No new matter is added.

Briefly recapitulating, amended independent Claim 1 is directed to a predetermined error vector magnitude reduction circuit. The circuit includes a) an inphase register for storing digital inphase bit patterns; b) a quadrature register for storing digital quadrature bit patterns; c) an inphase digital-to-analog converter (DAC) for converting the digital inphase

[1] Specification, page 12, line 6 and page 11, line 16.

bit patterns to an inphase analog signal; d) a quadrature DAC for converting the digital quadrature bit patterns to a quadrature analog signal; and e) at least one lookup table containing predetermined digital inphase and quadrature bit patterns for comparison with the digital inphase and quadrature bit patterns stored in the inphase and quadrature registers. The at least one lookup table also contains modified inphase and quadrature analog data that do not cause overshoot. The modified inphase and quadrature analog data replace the inphase and quadrature analog signals at the output of the DACs when there is a match between the predetermined digital inphase and quadrature bit patterns stored in the lookup table and the digital inphase and quadrature bit patterns stored in the inphase and quadrature registers. Independent Claim 9 is directed to an alternative embodiment, also reciting modified inphase and quadrature analog signals that do not cause overshoot. With Applicants' invention, improved communications performance is achieved through reduced overshoot.[2]

Original independent Claim 14 is directed to a transmitter comprising a baseband processor for generating inphase and quadrature digital bit patterns; and a predetermined error vector magnitude (EVM) reduction circuit for converting the inphase and quadrature digital bit patterns to analog signals that minimize EVM by correlating the inphase and quadrature digital bit patterns to known EVM scatter patterns. The transmitter also includes a mixing stage for mixing the analog signal up to an RF signal; a power amplifier for amplifying the RF signal; and an antenna for transmitting the RF signal.

Original independent Claim 20 is directed to a method for predetermined error vector magnitude reduction. The method includes a step of testing to detect overshoot in transitions from one phase state to another at the output of a transmitter; a step of correlating the overshoot to particular error vector magnitude scatter patterns; and a step of correlating the scatter patterns to particular inphase and quadrature bit patterns. The method also includes a

[2] Specification, page 5, lines 10-30.

step of forming a lookup table containing the predetermined inphase and quadrature bit patterns and modified inphase and quadrature data for each of the bit patterns that does not cause overshoot; and a step of using the lookup table to prevent or reduce error vector magnitude at the output of the transmitter.

Park discloses a device for linarizing a transmitter, where the device includes a predistortion lookup table containing data to compensate for transmitter distortion characteristics.[3] In the outstanding Office Action, the baseband filters 201 and 203 in Fig. 7 of Park are identified as corresponding to the "inphase register" and "quadrature register" recited in Claim 1, respectively. In Claim 1, the inphase register stores digital inphase bit patterns, and the quadrature register stores digital quadrature bit patterns. On the other hand, operation of the baseband filters 201 and 203 predistort the input data IchD and QchD according to the filter coefficients IFC and QFC.[4] However, Park does not disclose or suggest that baseband filters 201 and 203 store the data IchD and QchD, respectively. Therefore, Applicants submit that baseband filters 201 and 203 do not correspond to Applicants' claimed "inphase register" and "quadrature register" as recited in Claim 1 of the present application.

Furthermore, Applicants' Claim 1 recites that "the modified inphase and quadrature analog data replaces the inphase and quadrature analog signals at the output of the DACs". The outstanding Office Action asserts that Applicants' claimed feature of replacing signals at the output of the DACs is disclosed in column 5, lines 22-35 of Park (which corresponds to Fig. 2 of Park). In Fig. 2 of Park, the data IPDD and QPDD are output from the memory 233, and the filter coefficient generator 235 generates the filter coefficients IFC and QFC based on the data IPDD and QPDD. The filter coefficients IFC and QFC are input to the baseband filters 201 and 203, respectively. However, as seen in Figure 2 of Park, the data IPDD and

[3] Park, abstract and Figure 7.
[4] Park, column 5, lines 36-43.

QPDD output from the memory 233 do not replace analog signals output from DACs 205 and 207. Thus, cited passages of Park do not disclose or suggest Applicants' claim of "the modified inphase and quadrature analog data replaces the inphase and quadrature analog signals at the output of the DACs."

Moreover, in Fig. 7 of Park, the analog signals output from the DACs 205 and 107, respectively, and the data IPDD and QPDD output from the memory 233 via the DAC 237 are multiplied by the multipliers 511 and 513.[5] Namely, the output of DAC 237 and the output of DACs 205 and 207 are multiplied, and thus for another reason it can be seen that the output of DAC 237 do not replace the output of DACs 205 and 207.

Applicants submit that Applicants' Claim 9 distinguishes over Park for substantially the same reasons as identified above relative to Claim 1. That is, the baseband filters 201 and 203 of Park do not correspond to "inphase register" and "quadrature register" recited in Applicants' Claim 9. Furthermore, Applicants' Claim 9 recites that "the modified inphase and quadrature bit patterns replace the digital inphase and quadrature bit patterns at the input of the DACs". The outstanding Office Action suggests that this feature of Claim 9 is disclosed in column 5, lines 22-35 of Park (corresponding to Figure 2 of Park). In Fig. 2 of Park, the data IPDD and QPDD are output from the memory 233, and the filter coefficient generator 235 generates the filter coefficients IFC and QFC based on the data IPDD and QPDD. The filter coefficients IFC and QFC are input to the baseband filters 201 and 203, respectively. The baseband filters 201 and 203 predistort the input data IchD and QchD according to the filter coefficients IFC and QFC.[6] However, as discussed above, in Fig. 2 of Park, the data IPDD and QPDD output from the memory 233 do not replace the digital data IchD and QchD at the input of DACs 205 and 207. Thus, Park does not disclose or suggest

[5] Park, column 13, lines 33-43.
[6] Park, column 5, lines 36-43.

Applicants' claimed "modified inphase and quadrature bit patterns [that] replace the digital inphase and quadrature bit patterns at the input of the DACs."

Applicants submit that amended independent Claim 17 distinguishes over Park for at least the reasons presented above relative to amended Claims 1 and 9.

Applicants' original Claim 14 recites that "EVM reduction circuit for converting the inphase and quadrature digital bit patterns to analog signals that minimize EVM by correlating the inphase and quadrature digital bit patterns to known EVM scatter patterns." In the outstanding Office Action, elements 201, 203, 205, 207, 511, 513, 209, 211, 229, 211, 233 and 237 shown in Fig. 7 of Park (corresponding to column 12, line 50 to column 13, line 67) are assert to be equivalent to Applicants' claimed "EVM reduction circuit". However, Applicants submit there is no mention of "EVM scatter pattern" in column 12, line 50 to column 13, line 67 of Park. In view of this failing, Applicants request the outstanding rejection of Claim 14 be withdrawn.

Applicants original Claim 20 recites a "step of testing to detect overshoot in transitions from one phase state to another phase state." Park discloses that the distortion characteristics of transmitter is measured in advance.[7] However, Park does not disclose or suggest Applicants' claimed step of testing. Furthermore, Claim 20 discloses a "step of correlating the overshoot to particular error vector magnitude scatter patterns" and a "step of correlating the scatter patterns to particular inphase and quadrature bit patters." In the passage of Park cited in the rejection of Claim 20,[8] there is no mention of "overshoot" and "error vector magnitude scatter patterns." While multipliers 511 and 513 shown in Fig. 7 of Park merely multiply the output of DACs 205 and 207 and the output of DAC 237, respectively. Multipliers 511 and 513 do not have the functions of "correlating the overshoot

[7] Park, column 13, lines 14-20.
[8] Park, column 12, line 50 to column 13, line 67.

to particular error vector magnitude scatter patterns" and "correlating the scatter patterns to particular inphase and quadrature bit patterns."

Because the cited reference does not disclose or suggest all the elements of independent Claims 1, 9, 14, 15, 17, and 20, Applicants submit the inventions defined by Claims 1, 9, 15, 17, and 20, and all claims depending therefrom, are not anticipated and are not rendered obvious by the asserted prior art for at least the reasons stated above.[9]

Accordingly, in view of the present amendment and in light of the previous discussion, Applicants respectfully submit that the present application is in condition for allowance and respectfully request an early and favorable action to that effect.

Respectfully submitted,

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[9] MPEP § 2142 "...the prior art reference (or references when combined) must teach or suggest **all** the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."